WHAT IS CLAIMED IS:

1. An integrated circuit driver comprising:

an output node for coupling to a load and providing a first voltage level at a predetermined impedance, the first voltage level corresponding to a logic high level, and providing a second voltage level at the predetermined impedance, the second voltage level corresponding to a logic low level, and presenting a high impedance state;

a first switched resistive element coupled to the output node and also coupled to a first voltage source;

a second switched resistive element coupled to the output node and also coupled to a ground potential;

a third switched resistive element coupled to the output node and also coupled to the ground potential;

a first control line coupled to the first switched resistive element, the first control line for actuating the first switched resistive element;

a second control line coupled to the second switched resistive element, the second control line for actuating the second switched resistive element; and

a third control line coupled to the third switched resistive element, the third control line for actuating the third switched resistive element;

wherein the load is a resistive load coupled to a third voltage source and the first voltage level, the second voltage level and the predetermined impedance remain substantially constant with variations in manufacturing process, variations in the first voltage source and variations in operating temperature.

2. The integrated circuit driver of claim 1 wherein the first switched resistive element comprises a PFET.

3. The integrated circuit driver of claim 1 wherein the second switched resistive element comprises an NFET.

4. The integrated circuit driver of claim 1 wherein the third switched resistive element comprises an NFET.

5. The integrated circuit driver of claim 1 wherein the ratio of the resistance of the second switched resistive element to the resistance of the third switched resistive element is approximately five to one.

6. The integrated circuit driver of claim 1 wherein the first voltage source is approximately 1.8 volts.

7. A method of communicating data in an integrated circuit using internal interconnects, the method comprising:

receiving a data signal;

adjusting a first resistance coupled to a first supply voltage, based on a manufacturing process, the first supply voltage and a temperature;

adjusting a second resistance coupled to a second supply voltage, based on the manufacturing process, the first supply voltage and the temperature; and

adjusting a third resistance coupled to the second supply voltage, based on the manufacturing process, the first supply voltage and the temperature.

8. A method of communicating data in an integrated circuit using internal interconnects, the method comprising:

selecting a resistance of a divider network based on a manufacturing process, a supply voltage and a temperature;

selecting an edge rate of a driver coupled to the divider network, the selected edge rate based on the manufacturing process, the supply voltage and the temperature;

receiving a data signal; and

providing an output based on the data signal, the resistance, and the edge rate.

9. The method of claim 8 wherein selecting an edge rate of a driver coupled to the divider network comprises maintaining a substantially constant edge rate.

10. The method of claim 8 wherein providing an output comprises turning on a PFET transistor and turning off an NFET transistor.

11. The method of claim 8 wherein selecting a resistance of a divider network comprises selecting a plurality of parallel resistance elements.

12. The method of claim 8 wherein selecting a resistance of a divider network comprises executing programming for selecting resistance elements from a plurality of switchable resistance elements.

13. The method of claim 8 wherein selecting an edge rate of a driver coupled to the divider network comprises selecting a plurality of parallel resistance elements.

14. The method of claim 8 wherein selecting an edge rate of a driver coupled to the divider network comprises executing programming for selecting resistance elements from a plurality of switchable resistance elements.

15. The method of claim 8 further comprising:

receiving a tristate enable signal; and

actuating a switchable resistance element in response to the tristate enable signal.

16. The method of claim 15 wherein actuating a switchable resistance element comprises actuating a programmable inverter.

17. A driver comprising:

an output section, including:

an output node;

a plurality of P-nodes;

a first plurality of P-channel transistors, each P-channel transistor of the first plurality of P-channel transistors having a source coupled to a supply voltage and a drain coupled to the output node, wherein each of the plurality of P-nodes is coupled to a gate of each P-channel transistor of the first plurality of P-channel transistors;

a plurality of N-nodes;

a first plurality of N-channel transistors, each N-channel transistor of the first plurality of N-channel transistors having a drain coupled to the output node and a source coupled to a ground potential relative to the supply voltage wherein each of the plurality of N-nodes is coupled to a gate of each N-channel transistor of the first plurality of N-channel transistors; and

a second plurality of N-channel transistors, each N-channel transistor of the second plurality of N-channel transistors having a drain coupled to the output node and a source coupled to the ground potential wherein each of the plurality of N-nodes is coupled to a gate of each N-channel transistor of the second plurality of N-channel transistors; and

a first predriver section including:

a P-output node;

a second plurality of P-channel transistors, each P-channel transistor of the second plurality of P-channel transistors having a source coupled to the supply voltage and a drain coupled to the P-output node, wherein each of the plurality of P-nodes is coupled to a gate of each P-channel transistor of the second plurality of P-channel transistors;

a third plurality of N-channel transistors, each N-channel transistor of the third plurality of N-channel transistors having a drain coupled to the P-output node and a source coupled to the ground potential and wherein each of the plurality of N-nodes is coupled to a gate of each N-channel transistor of the third plurality of N-channel transistors;

an N-output node;

a third plurality of P-channel transistors, each P-channel transistor of the third plurality of P-channel transistors having a source coupled to the supply voltage and a drain coupled to the N-output node, wherein each of the plurality of P-nodes is coupled to a gate of each P-channel transistor of the third plurality of P-channel transistors; and

a fourth plurality of N-channel transistors, each N-channel transistor of the fourth plurality of N-channel transistors having a drain coupled to the N-output node and a source coupled to the ground potential and wherein each of the plurality of N-nodes is coupled to a gate of each N-channel transistor of the fourth plurality of N-channel transistors; and

wherein the P-output node is coupled to the source of each P-channel transistor of the first plurality of P-channel transistors and further wherein the N-output node is coupled to the source of each N-channel transistor of the first plurality of N-channel transistors; and

a second predriver section including:

a T-node;

a fourth plurality of P-channel transistors, each P-channel transistor of the fourth plurality of P-channel transistors having a source coupled to the supply voltage and a drain coupled to the T-node, wherein each of the plurality of P-nodes is coupled to a gate of each P-channel transistor of the fourth plurality of P-channel transistors; and

a fifth plurality of N-channel transistors, each N-channel transistor of the fifth plurality of N-channel transistors having a drain coupled to the T-node and a source coupled to the ground potential and wherein each of the plurality of N-nodes is coupled to a gate of each N-channel transistor of the fifth plurality of N-channel transistors; and

wherein the T-node is coupled to the source of each of the second plurality of N-channel transistors of the output section.

18. The driver of claim 17 wherein the P-channel transistors are PFET transistors and wherein the N-channel transistors are NFET transistors.

19. The driver of claim 17 wherein the first plurality of P-channel transistors comprises one P-channel transistor having an effective resistance lower than an effective resistance of each of the other P-channel transistors in the first plurality of P-channel transistors.

20. The driver of claim 17 wherein the first plurality of N-channel transistors comprises one N-channel transistor having an effective resistance lower than an effective resistance of each of the other N-channel transistors in the first plurality of N-channel transistors.

21. The driver of claim 17 wherein the second plurality of N-channel transistors comprises one N-channel transistor having an effective resistance lower than an effective resistance of each of the other N-channel transistors in the second plurality of N-channel transistors.

22. The driver of claim 17 wherein the ratio of the effective resistance of the second plurality of N-channel transistors to the effective resistance of the first plurality of N-channel transistors is approximately five to one.

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